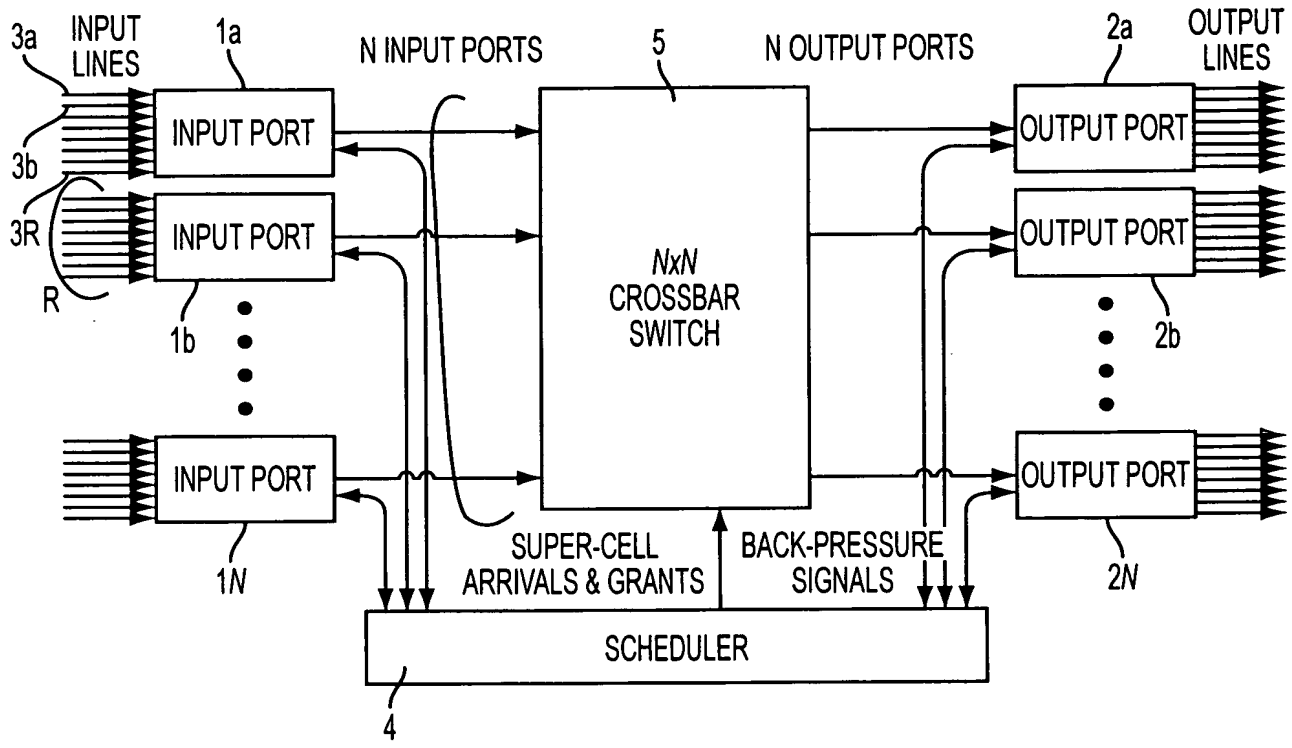


FIG. 1

PARAMETER	MEANING	TYPICAL VALUE
N	NUMBER OF INPUT AND OUTPUT PORTS	64
L	NUMBER OF INPUT AND OUTPUT LINES	512
R	NUMBER OF LINES PER PORT	8
K	NUMBER OF CLASSES	8
M	NUMBER OF SCHEDULING MODULES	16
S	NUMBER OF PIPELINE STAGES PER SCHEDULING MODULE	1
C	NUMBER OF CELLS PER SUPER-CELL	8

FIG. 2

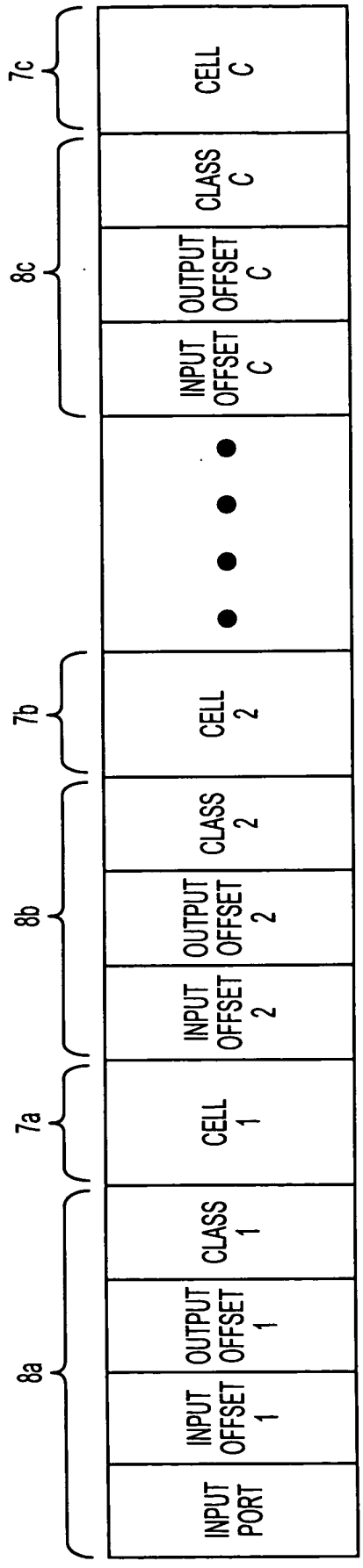

8a
INPUT PORT
INPUT OFFSET 1
OUTPUT OFFSET 1
CLASS 1
7a
CELL 1
8b
INPUT OFFSET 2
OUTPUT OFFSET 2
CLASS 2
7b
CELL 2
8c
INPUT OFFSET C
OUTPUT OFFSET C
CLASS C
7c
CELL C

FIG. 3

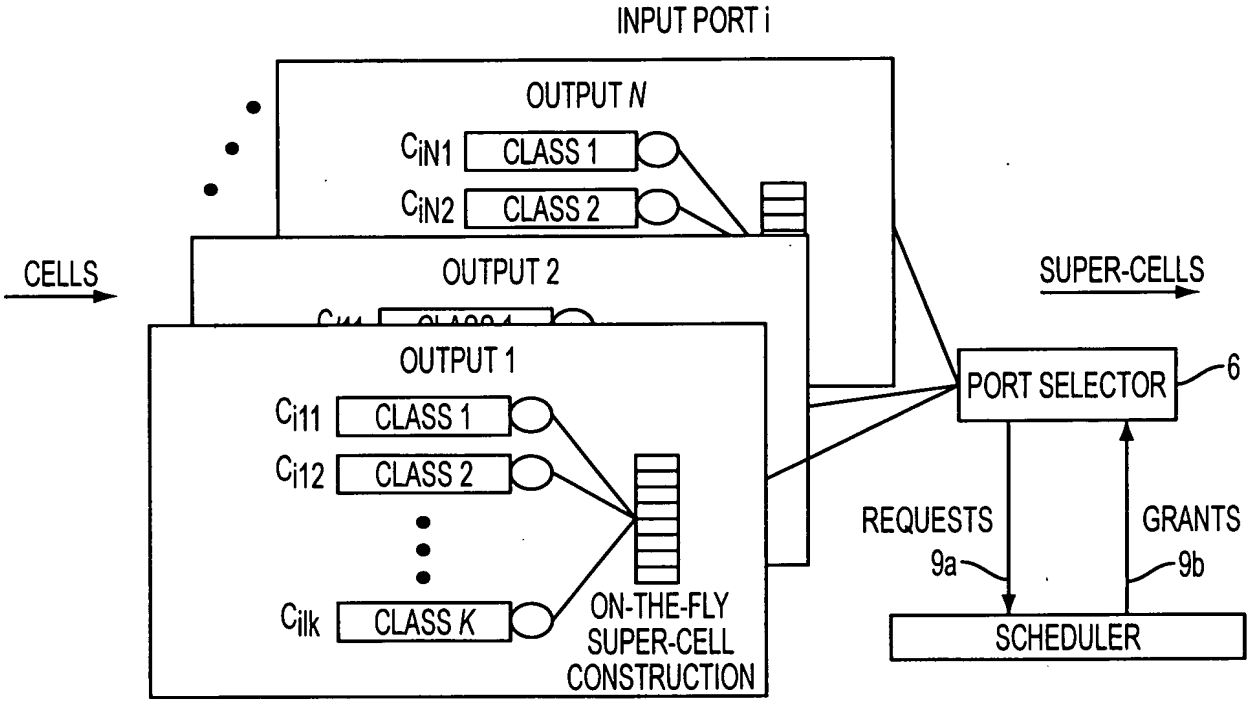

INPUT PORT i
OUTPUT N
C_{iN1}
CLASS 1
C_{iN2}
CLASS 2
CELLS
OUTPUT 2
SUPER-CELLS
OUTPUT 1
PORT SELECTOR
6
C_{i11}
CLASS 1
C_{i12}
CLASS 2
REQUESTS
9a
GRANTS
9b
C_{ilk}
CLASS K
ON-THE-FLY
SUPER-CELL
CONSTRUCTION
SCHEDULER

FIG. 4

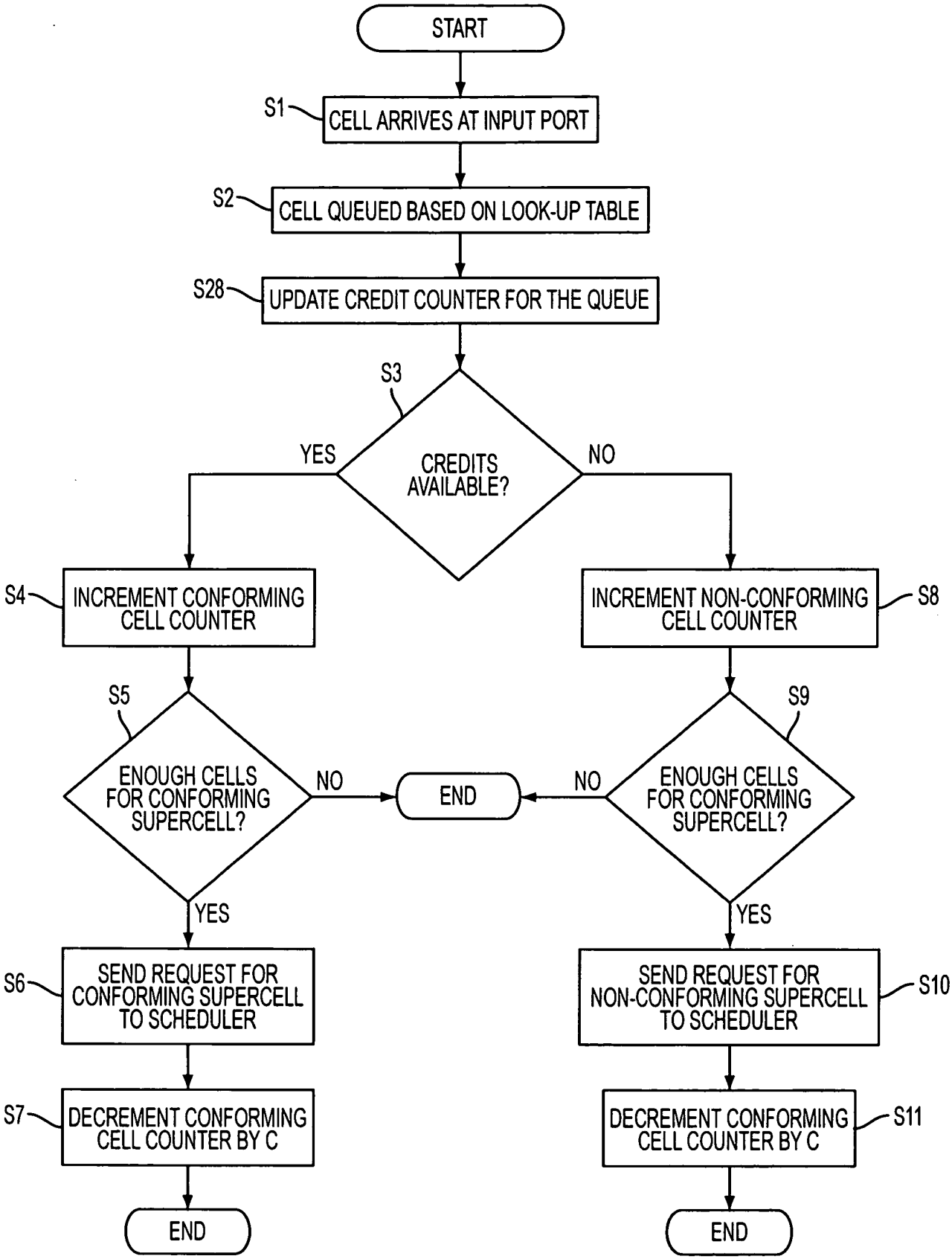

START
S1
CELL ARRIVES AT INPUT PORT
S2
CELL QUEUED BASED ON LOOK-UP TABLE
S28
UPDATE CREDIT COUNTER FOR THE QUEUE
S3
CREDITS AVAILABLE?
YES
NO
S4
INCREMENT CONFORMING CELL COUNTER
S8
INCREMENT NON-CONFORMING CELL COUNTER
S5
ENOUGH CELLS FOR CONFORMING SUPERCELL?
NO
END
NO
S9
ENOUGH CELLS FOR CONFORMING SUPERCELL?
YES
YES
S6
SEND REQUEST FOR CONFORMING SUPERCELL TO SCHEDULER
S10
SEND REQUEST FOR NON-CONFORMING SUPERCELL TO SCHEDULER
S7
DECREMENT CONFORMING CELL COUNTER BY C
S11
DECREMENT CONFORMING CELL COUNTER BY C
END
END

FIG. 5A

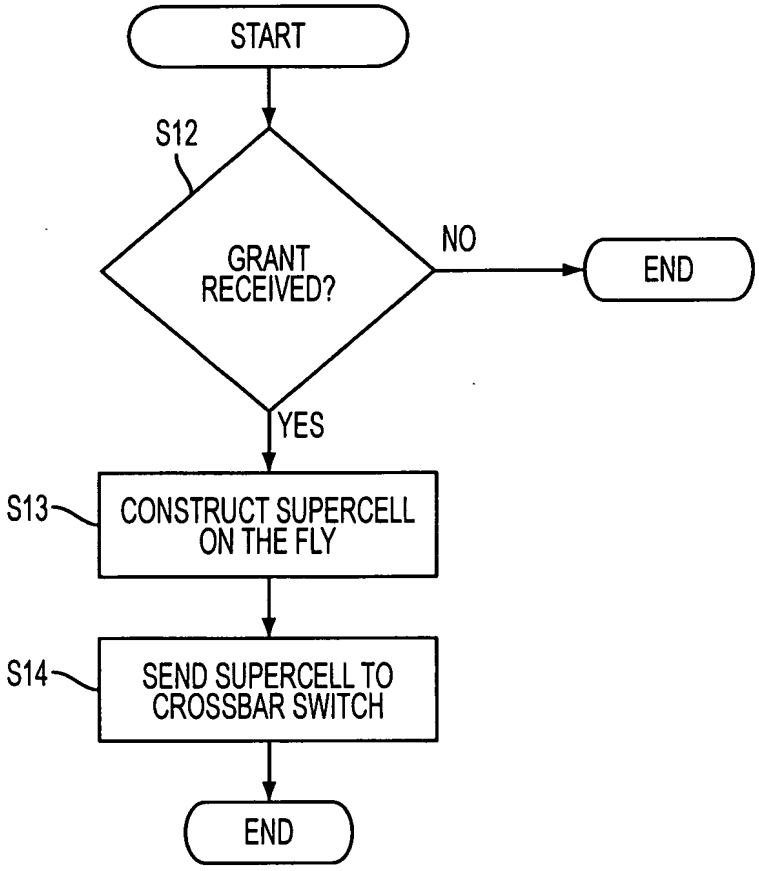

START
S12
GRANT RECEIVED?
NO
END
YES
S13
CONSTRUCT SUPERCELL ON THE FLY
S14
SEND SUPERCELL TO CROSSBAR SWITCH
END

FIG. 5B

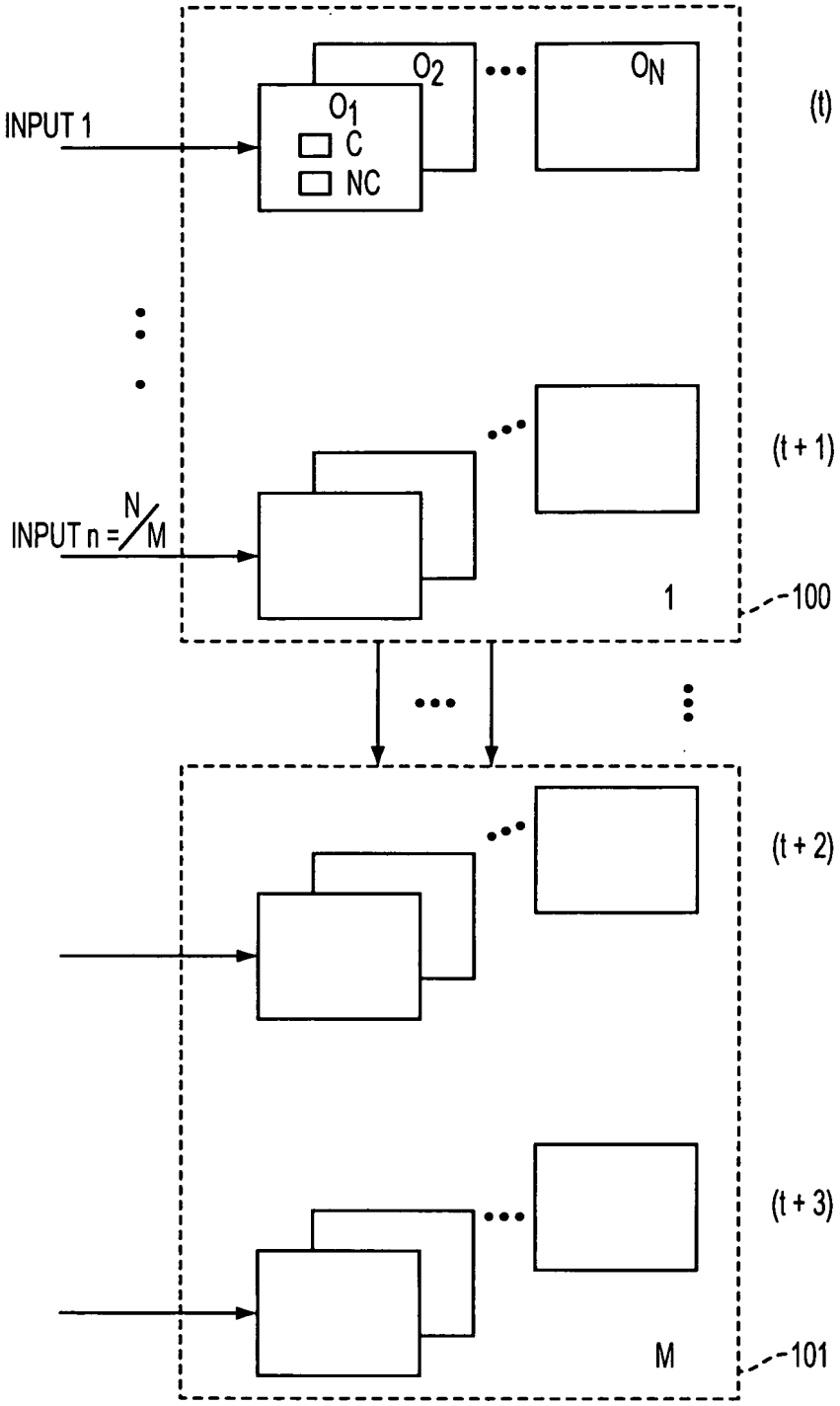


FIG. 6

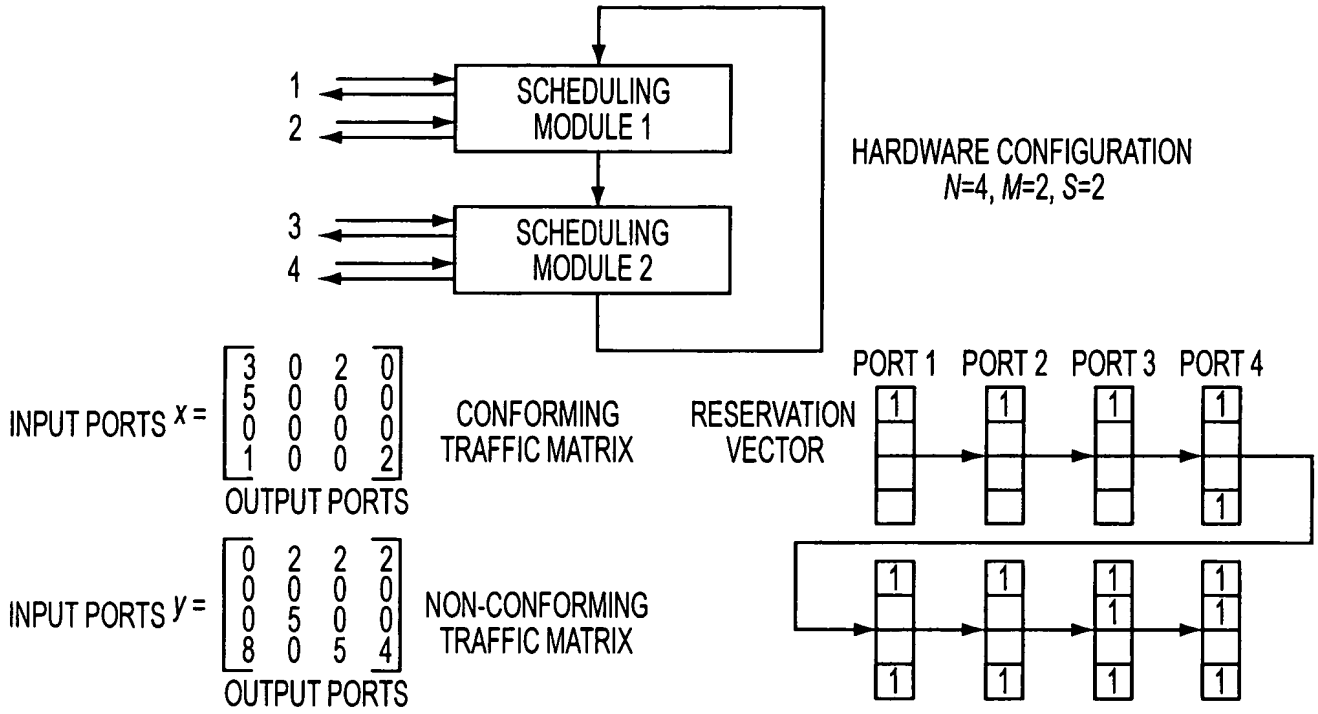

1
2
SCHEDULING MODULE 1
3
4
SCHEDULING MODULE 2
HARDWARE CONFIGURATION
N=4, M=2, S=2
INPUT PORTS x =
3 0 2 0
5 0 0 0
0 0 0 0
1 0 0 2
OUTPUT PORTS
CONFORMING TRAFFIC MATRIX
RESERVATION VECTOR
PORT 1
PORT 2
PORT 3
PORT 4
INPUT PORTS y =
0 2 2 2
0 0 0 0
0 5 0 0
8 0 5 4
OUTPUT PORTS
NON-CONFORMING TRAFFIC MATRIX

FIG. 7

MODULES	M1		DELAY	M2		DELAY	M3		DELAY	M4		DELAY
STAGES	s1	s2		s3	s4		s5	s6		s7	s8	
PORTS	p1 p2 p3 p4	p5 p6 p7 p8		p9 p10 p11 p12	p13 p14 p15 p16		p17 p18 p19 p20	p21 p22 p23 p24		p25 p26 p27 p28	p29 p30 p31 p32	
TIME SLOTS ↓	13 1	14 2	15 3	16 4	17 5	18 6	19 7	20 8	21 9	22 10	23 11	24 12
	24 12	13 1	14 2	15 3	16 4	17 5	18 6	19 7	20 8	21 9	22 10	23 11
	23 11	24 12	13 1	14 2	15 3	16 4	17 5	18 6	19 7	20 8	21 9	22 10
	22 10	23 11	24 12	13 1	14 2	15 3	16 4	17 5	18 6	19 7	20 8	21 9
	21 9	22 10	23 11	24 12	13 1	14 2	15 3	16 4	17 5	18 6	19 7	20 8
	20 8	21 9	22 10	23 11	24 12	13 1	14 2	15 3	16 4	17 5	18 6	19 7
	19 7	20 8	21 9	22 10	23 11	24 12	13 1	14 2	15 3	16 4	17 5	18 6
	18 6	19 7	20 8	21 9	22 10	23 11	24 12	13 1	14 2	15 3	16 4	17 5
	17 5	18 6	19 7	20 8	21 9	22 10	23 11	24 12	13 1	14 2	15 3	16 4
	16 4	17 5	18 6	19 7	20 8	21 9	22 10	23 11	24 12	13 1	14 2	15 3
	15 3	16 4	17 5	18 6	19 7	20 8	21 9	22 10	23 11	24 12	13 1	14 2
	14 2	15 3	16 4	17 5	18 6	19 7	20 8	21 9	22 10	23 11	24 12	13 1

FIG. 8

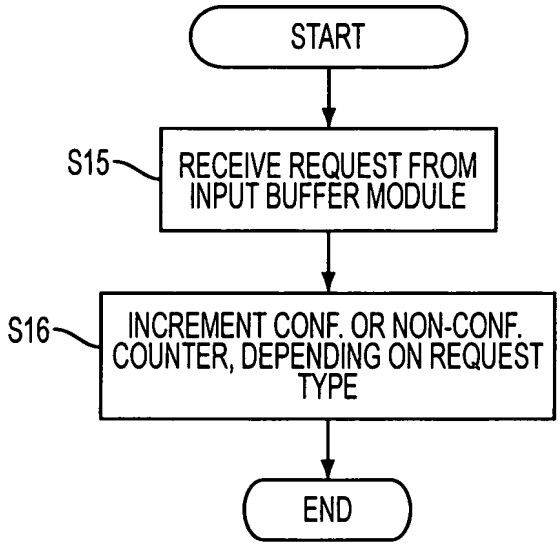

START
S15
RECEIVE REQUEST FROM INPUT BUFFER MODULE
S16
INCREMENT CONF. OR NON-CONF. COUNTER, DEPENDING ON REQUEST TYPE
END

FIG. 9

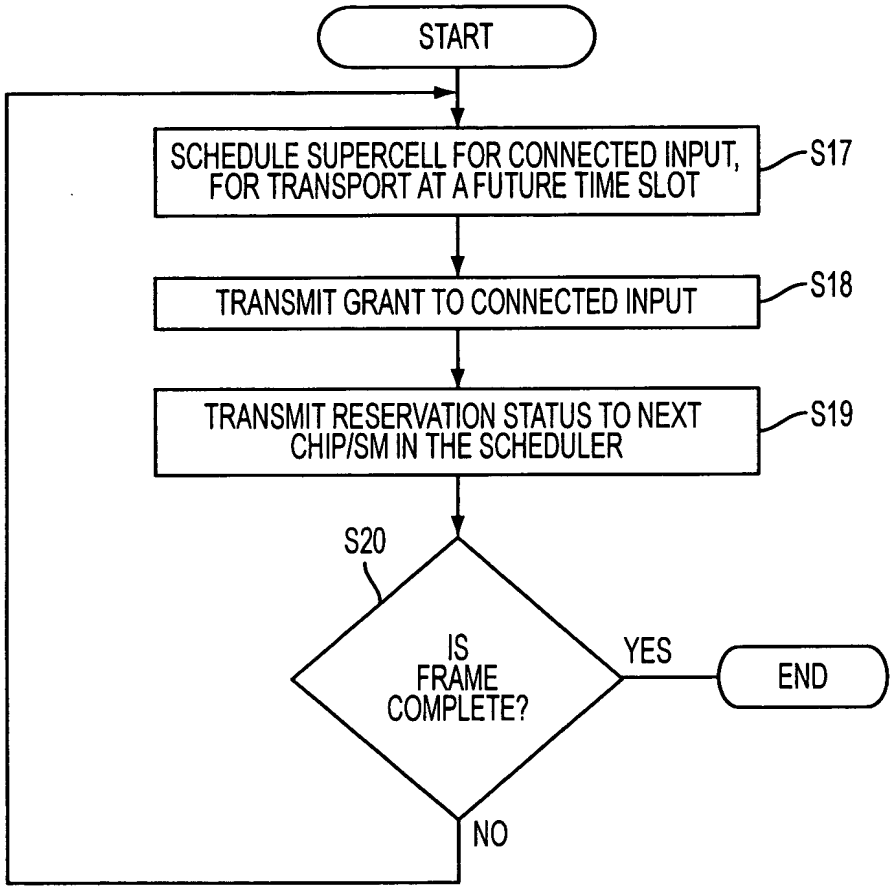
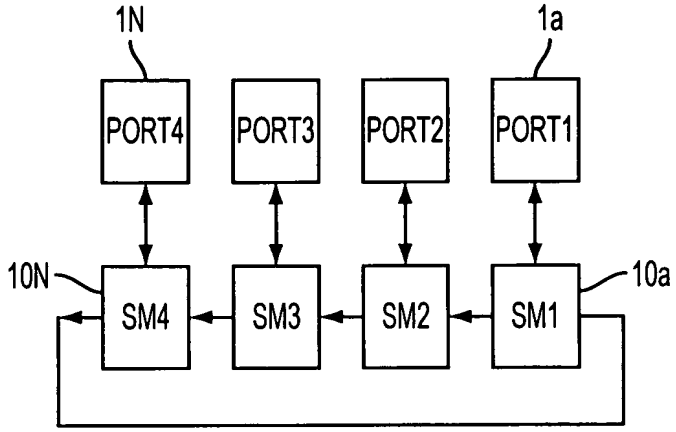

START
SCHEDULE SUPERCELL FOR CONNECTED INPUT, FOR TRANSPORT AT A FUTURE TIME SLOT
S17
TRANSMIT GRANT TO CONNECTED INPUT
S18
TRANSMIT RESERVATION STATUS TO NEXT CHIP/SM IN THE SCHEDULER
S19
S20
IS FRAME COMPLETE?
YES
END
NO

FIG. 10


1N
1a
PORT4
PORT3
PORT2
PORT1
10N
10a
SM4
SM3
SM2
SM1

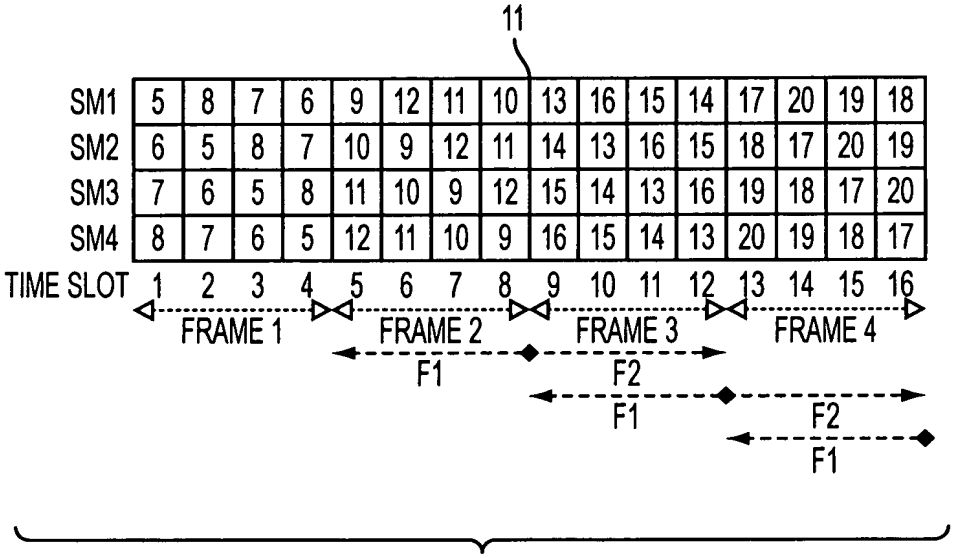

11
SM1 5 8 7 6 9 12 11 10 13 16 15 14 17 20 19 18
SM2 6 5 8 7 10 9 12 11 14 13 16 15 18 17 20 19
SM3 7 6 5 8 11 10 9 12 15 14 13 16 19 18 17 20
SM4 8 7 6 5 12 11 10 9 16 15 14 13 20 19 18 17
TIME SLOT 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
FRAME 1
FRAME 2
FRAME 3
FRAME 4
F1
F2
F1
F2
F1

FIG. 11

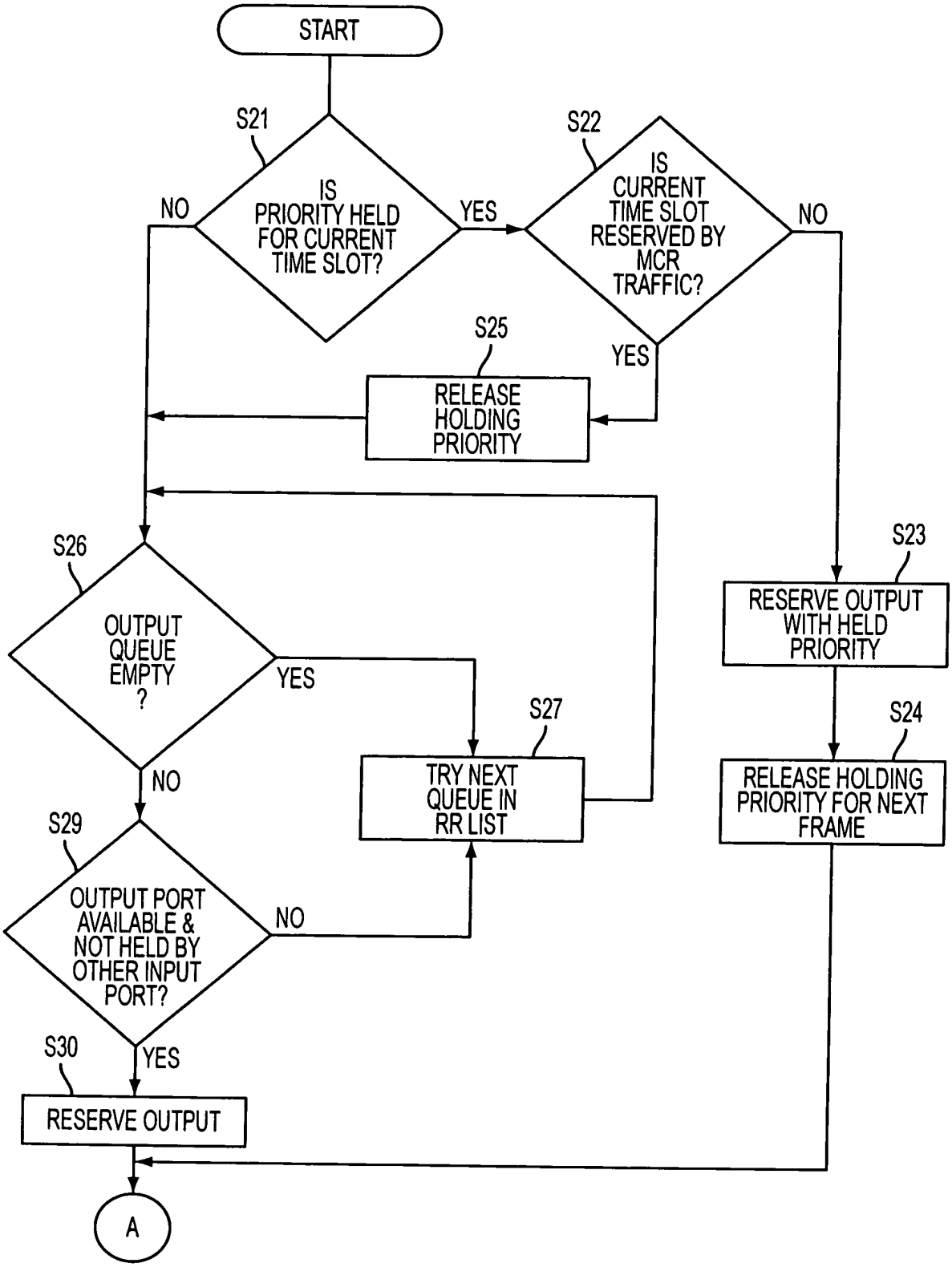

START
S21
IS PRIORITY HELD FOR CURRENT TIME SLOT?
NO
YES
S22
IS CURRENT TIME SLOT RESERVED BY MCR TRAFFIC?
NO
YES
S25
RELEASE HOLDING PRIORITY
S26
OUTPUT QUEUE EMPTY ?
YES
NO
S27
TRY NEXT QUEUE IN RR LIST
S29
OUTPUT PORT AVAILABLE & NOT HELD BY OTHER INPUT PORT?
NO
YES
S30
RESERVE OUTPUT
A
S23
RESERVE OUTPUT WITH HELD PRIORITY
S24
RELEASE HOLDING PRIORITY FOR NEXT FRAME

FIG. 12A

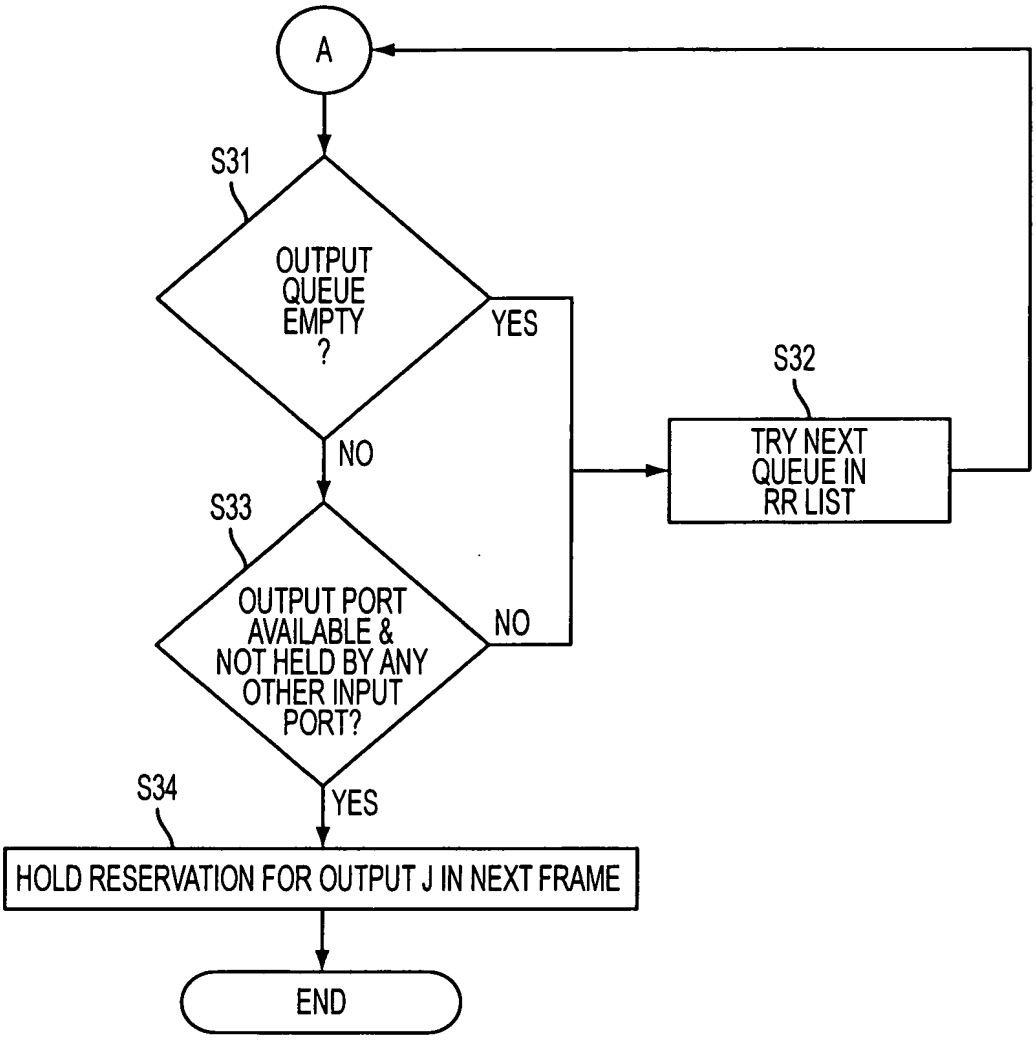

A
S31
OUTPUT QUEUE EMPTY ?
YES
NO
S32
TRY NEXT QUEUE IN RR LIST
S33
OUTPUT PORT AVAILABLE & NOT HELD BY ANY OTHER INPUT PORT?
NO
YES
S34
HOLD RESERVATION FOR OUTPUT J IN NEXT FRAME
END

FIG. 12B

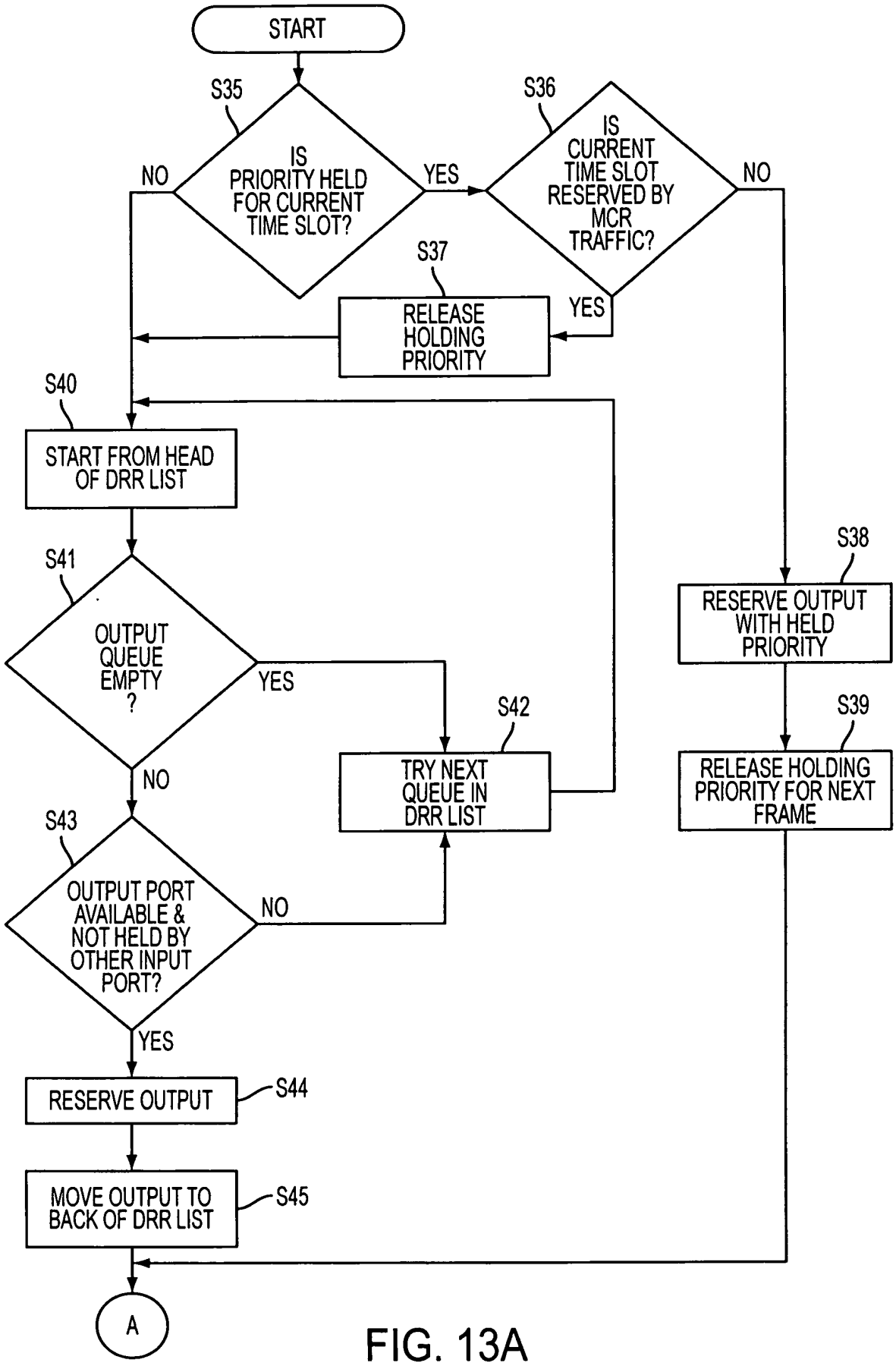

START
S35
IS PRIORITY HELD FOR CURRENT TIME SLOT?
NO
YES
S36
IS CURRENT TIME SLOT RESERVED BY MCR TRAFFIC?
NO
YES
S37
RELEASE HOLDING PRIORITY
S40
START FROM HEAD OF DRR LIST
S41
OUTPUT QUEUE EMPTY ?
YES
NO
S42
TRY NEXT QUEUE IN DRR LIST
S43
OUTPUT PORT AVAILABLE & NOT HELD BY OTHER INPUT PORT?
NO
YES
S44
RESERVE OUTPUT
S45
MOVE OUTPUT TO BACK OF DRR LIST
A
S38
RESERVE OUTPUT WITH HELD PRIORITY
S39
RELEASE HOLDING PRIORITY FOR NEXT FRAME

FIG. 13A

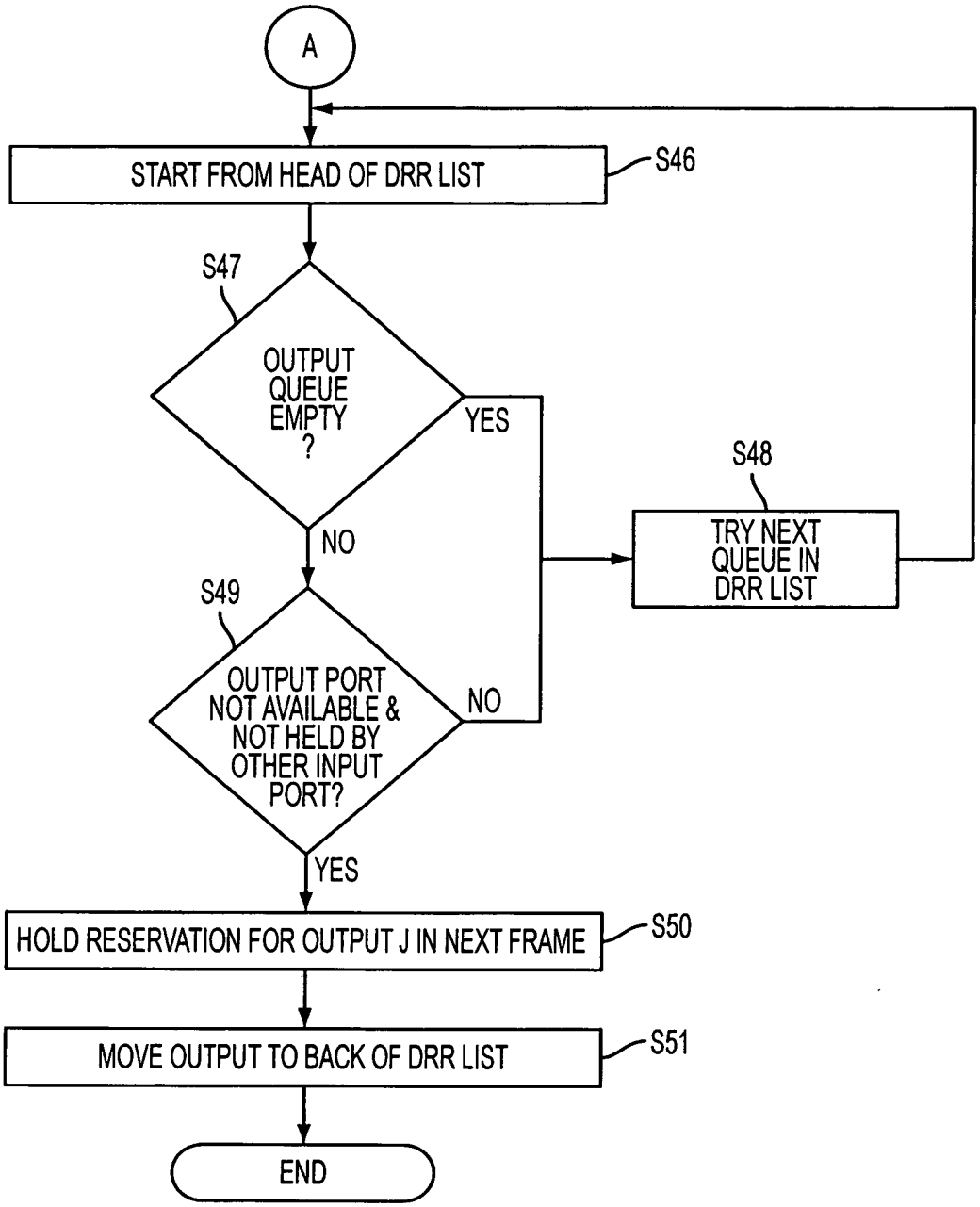

A
START FROM HEAD OF DRR LIST
S46
S47
OUTPUT QUEUE EMPTY ?
YES
NO
S48
TRY NEXT QUEUE IN DRR LIST
S49
OUTPUT PORT NOT AVAILABLE & NOT HELD BY OTHER INPUT PORT?
NO
YES
HOLD RESERVATION FOR OUTPUT J IN NEXT FRAME
S50
MOVE OUTPUT TO BACK OF DRR LIST
S51
END

FIG. 13B

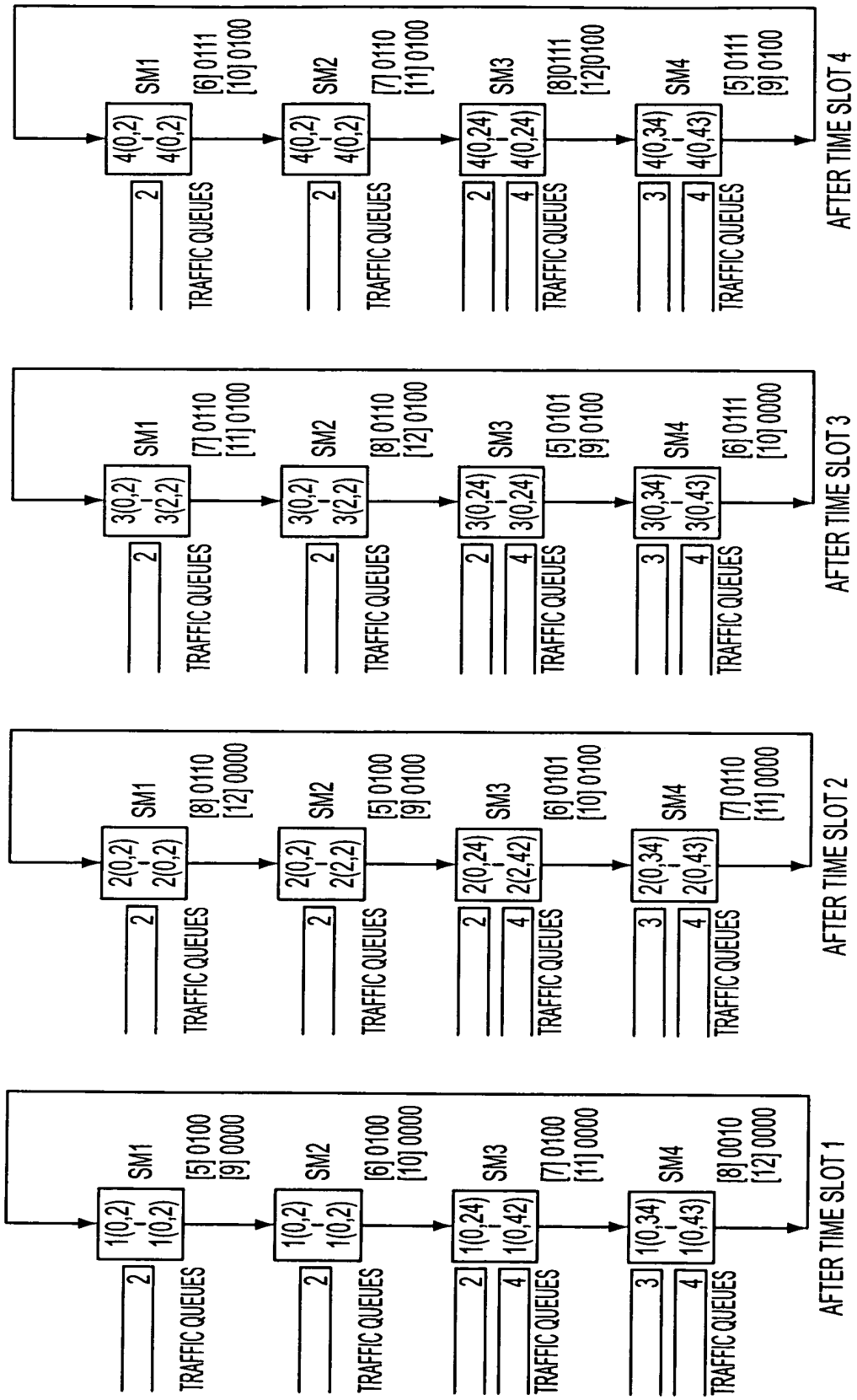

AFTER TIME SLOT 1
SM1
1(0,2)
1(0,2)
[5] 0100
[9] 0000
SM2
1(0,2)
1(0,2)
[6] 0100
[10] 0000
SM3
1(0,24)
1(0,42)
[7] 0100
[11] 0000
SM4
1(0,34)
1(0,43)
[8] 0010
[12] 0000
TRAFFIC QUEUES
2
2
2
4
3
4
AFTER TIME SLOT 2
SM1
2(0,2)
2(0,2)
[8] 0110
[12] 0000
SM2
2(0,2)
2(2,2)
[5] 0100
[9] 0100
SM3
2(0,24)
2(2,42)
[6] 0101
[10] 0100
SM4
2(0,34)
2(0,43)
[7] 0110
[11] 0000
AFTER TIME SLOT 3
SM1
3(0,2)
3(2,2)
[7] 0110
[11] 0100
SM2
3(0,2)
3(2,2)
[8] 0110
[12] 0100
SM3
3(0,24)
3(0,24)
[5] 0101
[9] 0100
SM4
3(0,34)
3(0,43)
[6] 0111
[10] 0000
AFTER TIME SLOT 4
SM1
4(0,2)
4(0,2)
[6] 0111
[10] 0100
SM2
4(0,2)
4(0,2)
[7] 0110
[11] 0100
SM3
4(0,24)
4(0,24)
[8]0111
[12]0100
SM4
4(0,34)
4(0,43)
[5] 0111
[9] 0100

FIG. 14A

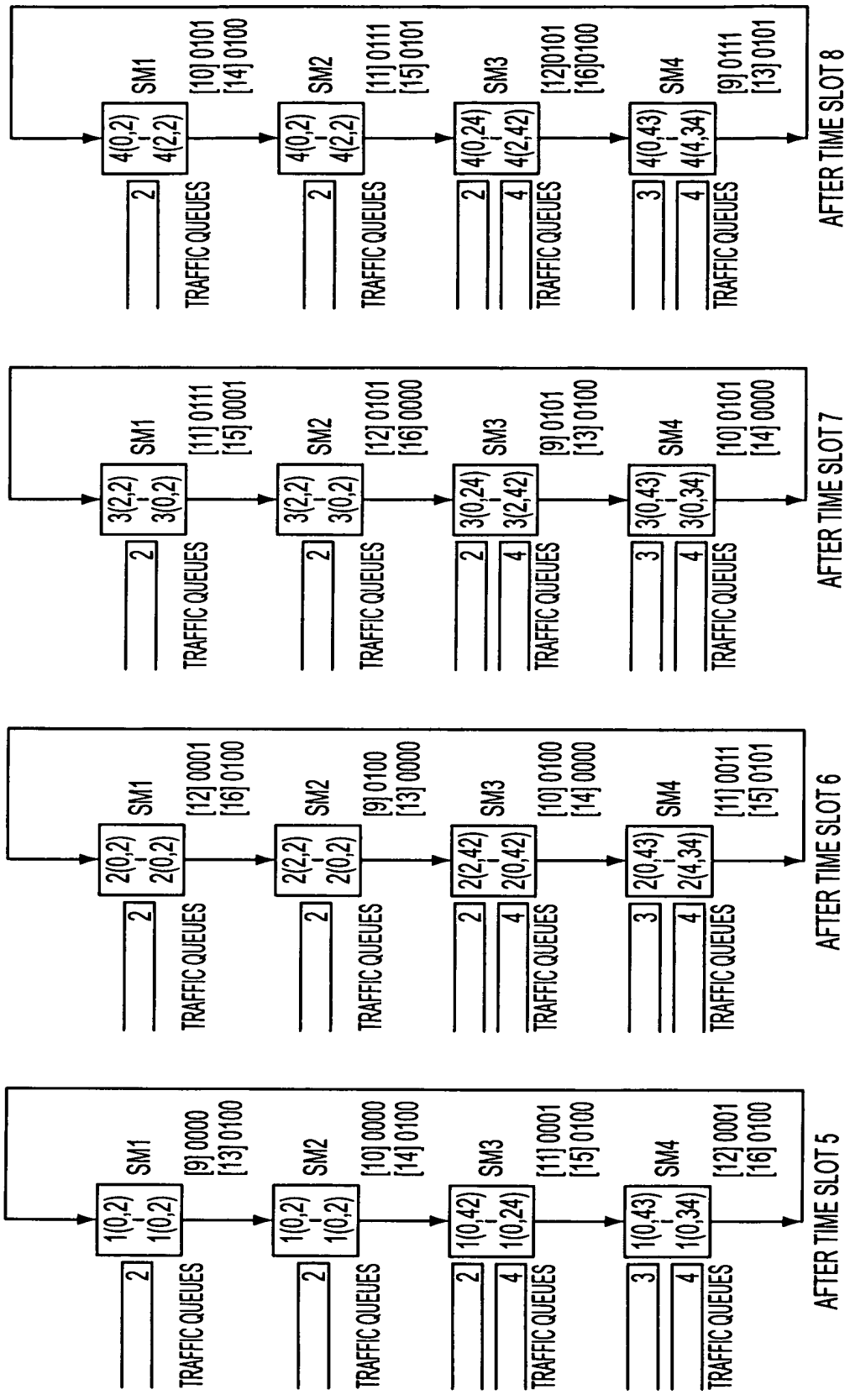

AFTER TIME SLOT 5
SM1
1(0,2)
1(0,2)
[9] 0000
[13] 0100
SM2
1(0,2)
1(0,2)
[10] 0000
[14] 0100
SM3
1(0,42)
1(0,24)
[11] 0001
[15] 0100
SM4
1(0,43)
1(0,34)
[12] 0001
[16] 0100
TRAFFIC QUEUES
2
2
2
4
3
4
AFTER TIME SLOT 6
SM1
2(0,2)
2(0,2)
[12] 0001
[16] 0100
SM2
2(2,2)
2(0,2)
[9] 0100
[13] 0000
SM3
2(2,42)
2(0,42)
[10] 0100
[14] 0000
SM4
2(0,43)
2(4,34)
[11] 0011
[15] 0101
AFTER TIME SLOT 7
SM1
3(2,2)
3(0,2)
[11] 0111
[15] 0001
SM2
3(2,2)
3(0,2)
[12] 0101
[16] 0000
SM3
3(0,24)
3(2,42)
[9] 0101
[13] 0100
SM4
3(0,43)
3(0,34)
[10] 0101
[14] 0000
AFTER TIME SLOT 8
SM1
4(0,2)
4(2,2)
[10] 0101
[14] 0100
SM2
4(0,2)
4(2,2)
[11] 0111
[15] 0101
SM3
4(0,24)
4(2,42)
[12]0101
[16]0100
SM4
4(0,43)
4(4,34)
[9] 0111
[13] 0101

FIG. 14B

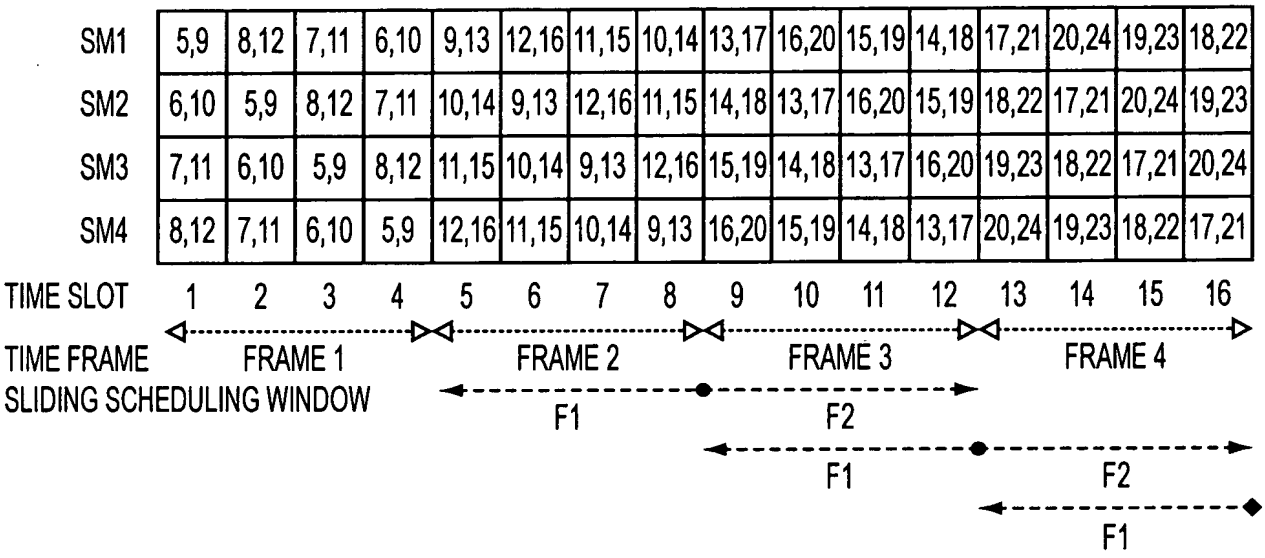

SM1 5,9 8,12 7,11 6,10 9,13 12,16 11,15 10,14 13,17 16,20 15,19 14,18 17,21 20,24 19,23 18,22
SM2 6,10 5,9 8,12 7,11 10,14 9,13 12,16 11,15 14,18 13,17 16,20 15,19 18,22 17,21 20,24 19,23
SM3 7,11 6,10 5,9 8,12 11,15 10,14 9,13 12,16 15,19 14,18 13,17 16,20 19,23 18,22 17,21 20,24
SM4 8,12 7,11 6,10 5,9 12,16 11,15 10,14 9,13 16,20 15,19 14,18 13,17 20,24 19,23 18,22 17,21
TIME SLOT 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
TIME FRAME
FRAME 1
FRAME 2
FRAME 3
FRAME 4
SLIDING SCHEDULING WINDOW
F1
F2
F1
F2
F1

FIG. 15

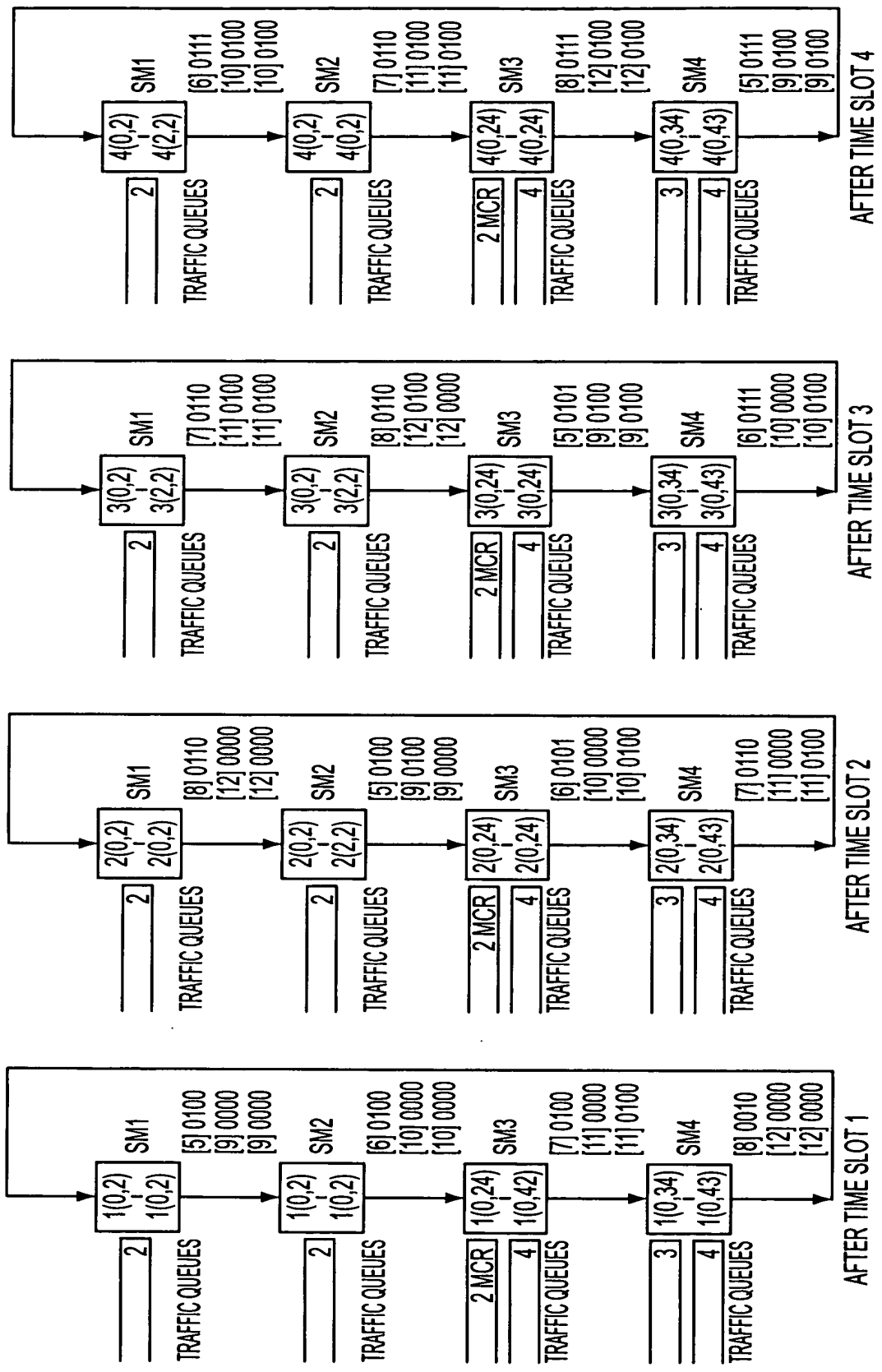

AFTER TIME SLOT 1
SM1
1(0,2)
1(0,2)
[5] 0100
[9] 0000
[9] 0000
SM2
1(0,2)
1(0,2)
[6] 0100
[10] 0000
[10] 0000
SM3
1(0,24)
1(0,42)
[7] 0100
[11] 0000
[11] 0100
SM4
1(0,34)
1(0,43)
[8] 0010
[12] 0000
[12] 0000
2
2 MCR
3
4
TRAFFIC QUEUES
AFTER TIME SLOT 2
SM1
2(0,2)
2(0,2)
[8] 0110
[12] 0000
[12] 0000
SM2
2(0,2)
2(2,2)
[5] 0100
[9] 0100
[9] 0000
SM3
2(0,24)
2(0,24)
[6] 0101
[10] 0000
[10] 0100
SM4
2(0,34)
2(0,43)
[7] 0110
[11] 0000
[11] 0100
AFTER TIME SLOT 3
SM1
3(0,2)
3(2,2)
[7] 0110
[11] 0100
[11] 0100
SM2
3(0,2)
3(2,2)
[8] 0110
[12] 0100
[12] 0000
SM3
3(0,24)
3(0,24)
[5] 0101
[9] 0100
[9] 0100
SM4
3(0,34)
3(0,43)
[6] 0111
[10] 0000
[10] 0100
AFTER TIME SLOT 4
SM1
4(0,2)
4(2,2)
[6] 0111
[10] 0100
[10] 0100
SM2
4(0,2)
4(0,2)
[7] 0110
[11] 0100
[11] 0100
SM3
4(0,24)
4(0,24)
[8] 0111
[12] 0100
[12] 0100
SM4
4(0,34)
4(0,43)
[5] 0111
[9] 0100
[9] 0100

FIG. 16

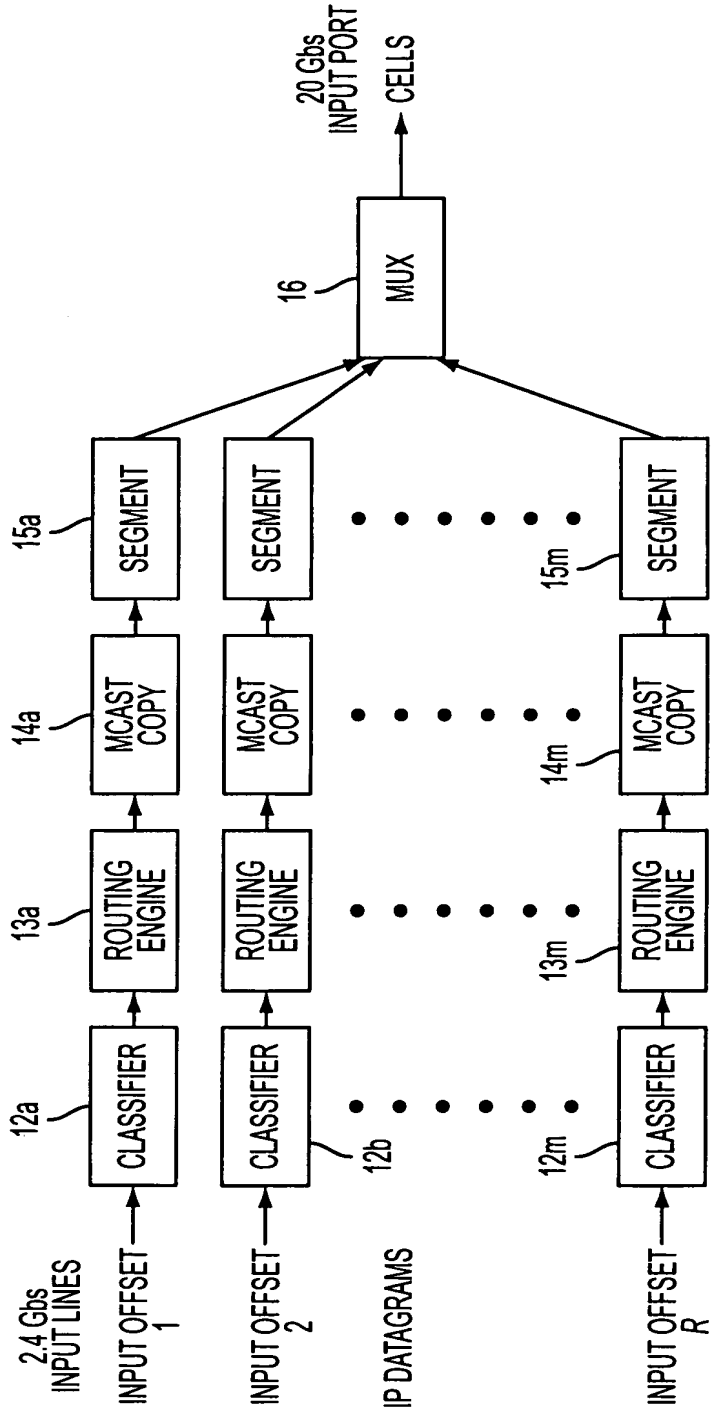

2.4 Gbs
INPUT LINES
INPUT OFFSET
1
INPUT OFFSET
2
IP DATAGRAMS
INPUT OFFSET
R
12a
12b
12m
CLASSIFIER
13a
13m
ROUTING
ENGINE
14a
14m
MCAST
COPY
15a
15m
SEGMENT
16
MUX
20 Gbs
INPUT PORT
CELLS

FIG. 17

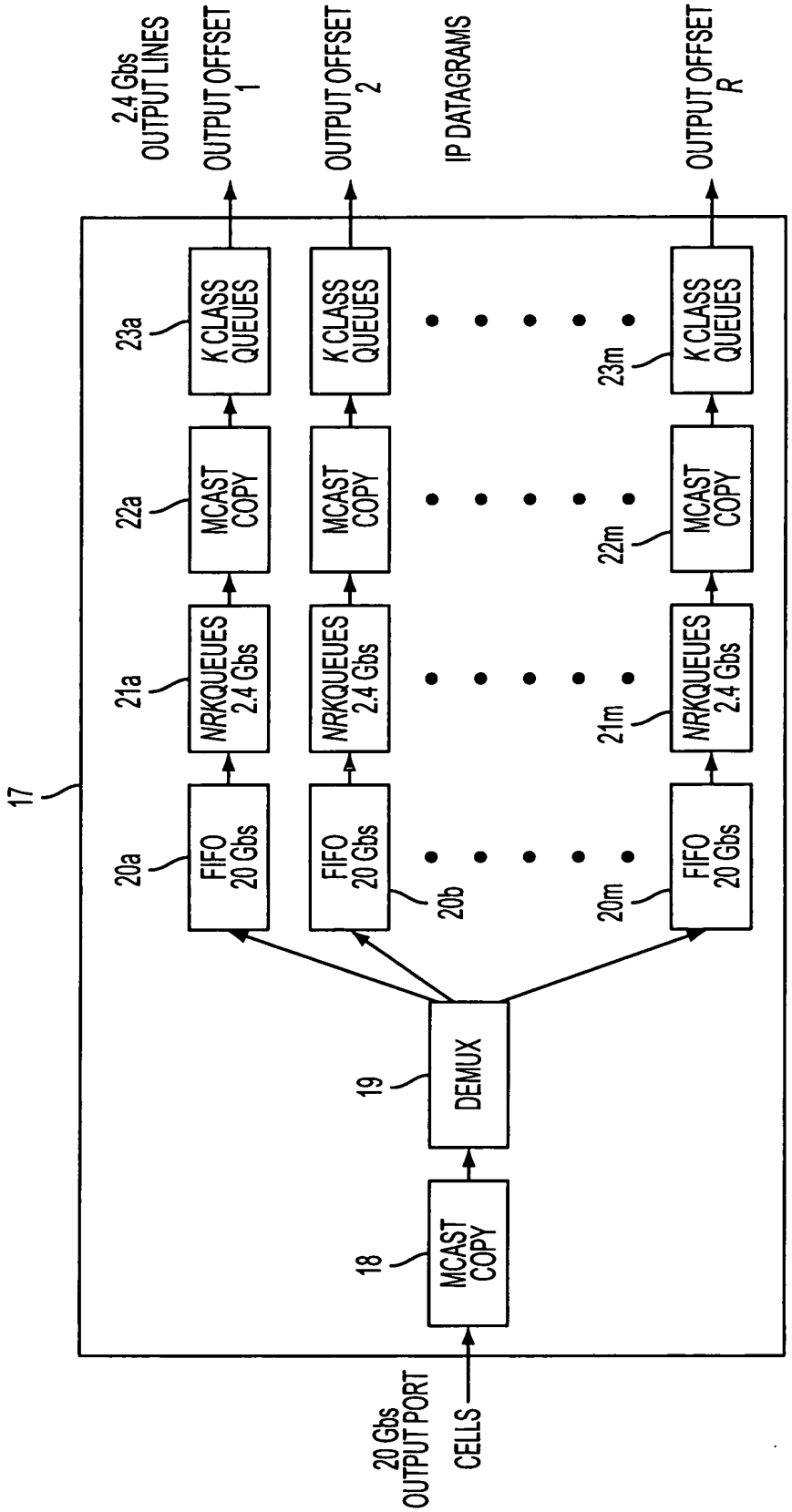

20 Gbs
OUTPUT PORT
CELLS
17
18
MCAST
COPY
19
DEMUX
20a
FIFO
20 Gbs
20b
20m
21a
NRKQUEUES
2.4 Gbs
21m
22a
MCAST
COPY
22m
23a
K CLASS
QUEUES
23m
IP DATAGRAMS
2.4 Gbs
OUTPUT LINES
OUTPUT OFFSET
1
OUTPUT OFFSET
2
OUTPUT OFFSET
R

FIG. 18